Monolithic-Like Heterogeneously Integrated Microsystems Using Dense Low-Loss Interconnects

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***Abstract* — In this paper, two integration technologies are discussed for heterogeneously integrated microsystems. First, this paper presents low-loss TSVs using an air-isolation technique for silicon interposers. The proposed air-isolated TSVs exhibit approximately 35% and 37% reduction in insertion loss and capacitance, respectively, at 20 GHz. Moreover, this paper presents a TSV-less integration technology using bridge chips and Compressible MicroInterconnects (CMIs). Compared to other packaging and assembly options, the investigated TSV-less approach provides monolithic-like electrical performance by significantly reducing chip-to-chip interconnect length and loss, increasing interconnect density, and providing the ability to seamlessly integrate chips of diverse functionalities.**

***Index Terms* — Compressible Interconnect, Heterogeneous Integration, Silicon interposer, Through-silicon-via.**

I. Introduction

The demand for high-bandwidth communication continues to grow in modern electronic systems [1], [2]. In particular, chip-to-chip interconnection is regarded as a key bottleneck to overall system performance and energy efficiency. To address these issues, heterogeneously integrated microsystems, in which multiple dice and/or passives are integrated within a single package, have been explored for digital, microwave/mm-wave, and mixed-signal systems [3], [4]. The proposed integration strategies include the vertical stacking of chips (3-D integration) and the lateral bonding of chips on an interposer substrate (2.5-D integration). While 3-D integration provides the shortest interconnection lengths, 2.5-D integration using interposers alleviates integration complexity by placing chips side-by-side on an interposer substrate. Such integrated microsystems improve electrical performance, such as bandwidth, latency, and I/O power, compared to conventional packages.

Through-silicon via (TSV) is a key enabling technology for such integrated microsystems [5]. However, TSVs exhibit relatively large insertion loss due to the lossy silicon substrate. To mitigate TSV loss, a number of technology innovations have been explored in the literature: for example, the use of polymers within silicon and glass substrates [6]—[8]. However, such approaches require new material integration, which may introduce new manufacturing considerations for research and development.

To this end, this paper presents two novel integration technologies for heterogeneously integrated microsystems. First, this paper discusses air-isolated TSVs, in which signal TSVs are partially isolated from neighboring TSVs using air to reduce TSV loss and parasitics in silicon interposers. Moreover, the paper proposes a TSV-less integration technology using bridge chips and dense mechanically compliant interconnects, which we refer to as Compressible MicroInterconnects (CMIs).

II. Heterogeneous System Integration Technologies

This section presents two technologies for heterogeneously integrated microsystems, as summarized in Fig. 1. The first schematic shows a conventional 2.5-D integration scheme of two chips stacked on a silicon interposer. This silicon interposer approach provides high-bandwidth communication between chips using high-density interconnects [2]. As illustrated in Fig. 1 (b), we can maintain the benefits of high-bandwidth communication but with the benefit of using low-loss TSVs achieved using air-isolation [9]. Moreover, this paper proposes a TSV-less and bridge-interconnect-based integration technology, as shown in Fig. 1 (c)

A. Air-isolated TSV technology for loss reduction in silicon interposers

This section describes the air-isolated low-loss TSVs [9]. In this approach, the signal TSVs are partially isolated from neighboring (signal or ground) TSVs using air. Figure 2 (a) shows an SEM image of air-isolated TSVs embedded in rectangular silicon pillars using a ground-signal-ground (GSG) configuration; two circular copper TSVs are embedded in each rectangular silicon pillar with copper traces. Thus, the signal and ground TSVs in the silicon pillars are partially isolated through air, as illustrated in the figure. TSV diameter, pitch, and height are 13 μm, 200 μm, and 320 μm, respectively, and the width, length, and height of the silicon pillars are 100 μm, 250 μm, and 220 μm, respectively.

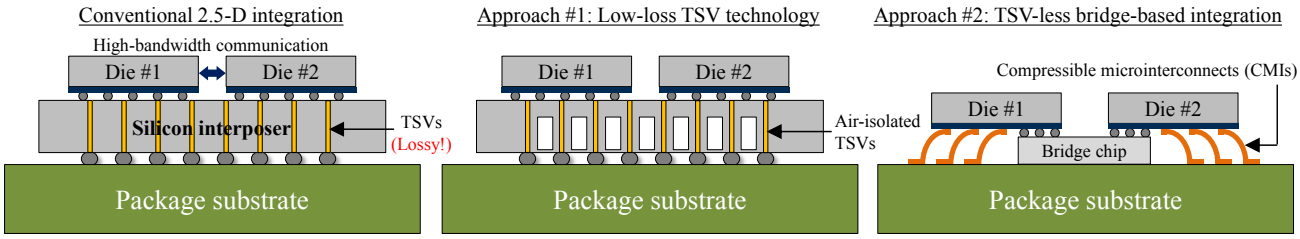


Fig 1. Three heterogeneously integrated microsystems: (a) conventional 2.5-D integration using a silicon interposer with TSVs, (b) low-loss silicon interposer using air-isolated TSVs, and (c) TSV-less and bridge-based integration technology using a bridge chip and CMIs.

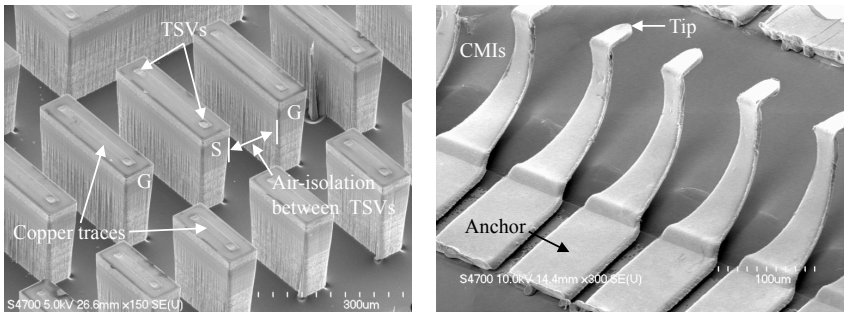


Fig 2. Two technology enablers for 2.5-D integration: (a) SEM image of air-isolated TSVs embedded in silicon pillars and (b) SEM image of concave-shaped CMIs.

To investigate the reduction in TSV loss and parasitics, the fabricated air-isolated TSVs are measured using a microprobe station and a Keysight PNA-N5245 network analyzer; the measurement results are compared with simulation results using Ansoft HFSS software. Moreover, to extract the loss of the GSG TSVs from a TSV-trace-TSV structure, the L-2L de-embedding technique [10] is performed using two copper trace lengths, as shown in Fig. 2 (a). Figure 3 shows the insertion loss and extracted capacitance of TSVs with and without air-isolation. The results show a 35% and 37% reduction in insertion loss and capacitance, respectively, at 20 GHz.

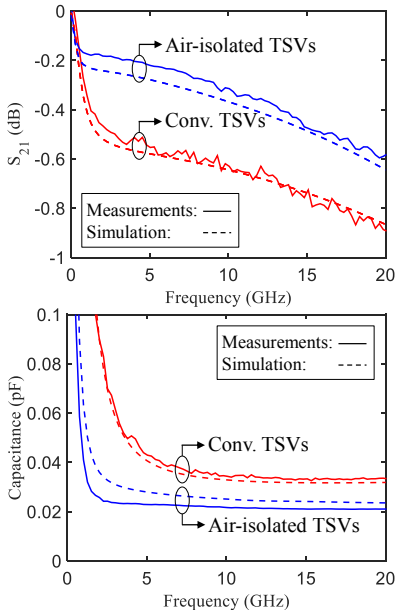
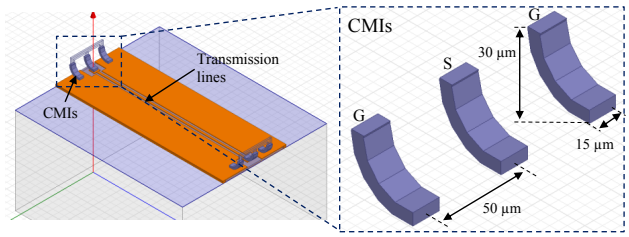


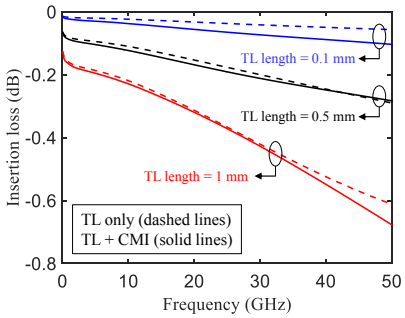
Fig. 3. Simulation and measurement results of air-isolated TSVs and conventional TSVs as a reference [9].

B. TSV-less bridge-based integration using CMIs

This section presents a TSV-less integration technology using a bridge chip and CMIs, as shown in Fig. 1 (c). First, please note the bridge chip can be formed using either silicon, glass, or possibly other substrates and is driven by application. In this approach, CMIs are a key enabler as they provide compressible vertical interconnection between ICs and the package, while a bridge chip provides broadband low-loss chip-to-chip communication. Figure 2 (b) illustrates an SEM image of concave-shaped CMIs. The stand-off height of the CMIs is 75 µm. The CMI length and in-line pitch are both 150 µm. Since CMIs are lithographically defined, CMIs can be easily miniaturized to have reduced I/O pad size and pitch. The CMI shown in the SEM achieves a 45 µm of vertical elastic deformation. This large deformation can compensate for any surface non-uniformity.



(a)



(b)

Fig. 4. (a) Simulation schematic of CMIs with transmission lines and (b) Simulation results of CMIs with transmission lines at the lengths of 0.1, 0.5, and 1 mm.

Figure 4 (a) illustrates the schematic of a 3-D link that consists of planar transmission lines (TLs) and CMIs on a bridge chip, in this case silicon. To analyze the total chip-to-chip signaling loss, the high-frequency loss of a CMI-TL-CMI structure is simulated using Ansoft HFSS software. A conductor-backed coplanar waveguide (CBCPW) structure is chosen for TLs to increase wiring density as well as to prevent any parasitic losses from the substrate. The signal width, spacing, and thickness of the TLs are 6 μm, 6 μm, and 2 μm, respectively; the thickness of the oxide liner between the signal trace and the ground plane is 3.5 μm. Figure 4 (b) illustrates the insertion loss of the 3-D link with the length of the transmission line as a variable. In the simulation, three transmission line lengths (0.1, 0.5, and 1mm) are compared. For the case of the longest transmission line (1 mm length), the total loss of the 3-D link (including 2 CMIs) is less than 0.7 dB; less than 10% of the loss occurs in the CMIs.

IV. Conclusion

This paper presents two integration technologies for heterogeneously integrated microsystems. First, air-isolated TSVs were presented to reduce TSV loss and parasitics in lossy silicon interposers. Using air-isolation between signal and ground TSVs, a reduction of approximately 35% and 37% in insertion loss and capacitance were achieved, respectively, at 20 GHz. Moreover, the paper explores a TSV-less integration technology using bridge chips and Compressible MicroInterconnects (CMIs). Such bridge-based interconnect technology provides monolithic-like electrical performance by significantly reducing chip-to-chip interconnect length and loss, increasing interconnect density, and providing the ability to seamlessly integrate chips of diverse functionalities.

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